Recursive Algorithm for Zero Skew Sub-Tree for Clock Gating Method

Ashok Kumar, C.[1]*, Dr. Madhavi, B, K.[2] and Dr. Lal Kishore, K[3]

1. Professor & Head, Dept. of ECE, TRR Engineering College, Hyderabad, AP, India
2. Professor, Dept. of ECE, Geetanjali College of Engg. & Tech., Hyderabad, AP, India
3. Vice-Chancellor, JNT University, Ananthapur, A.P, India

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Abstract: *Clock gating methods recently gained attention as a way of reducing power dissipation in digital circuits. In a typical synchronous circuit, especially in a general-purpose microprocessor, only a portion of the circuit is active at any given time. In this paper we present a zero-skew clock routing algorithm. The results have been verified with accurate waveform simulation. A recursive bottom-up algorithm is then applied for interconnecting two zero-skewed subtrees to a new tree with zero skew. The algorithm can be applied to single-staged clock trees, multistage clock trees, and multi-chip system clock trees.*